ABSTRACT

Roughly described, therefore, in accordance with a preferred embodiment of the present invention, a method is provided for fabricating an N-bit memory device with self-aligned buried diffusion implants and two isolated ONO segments in one cell. The method includes the steps of forming an ONO layer on a substrate, depositing a polysilicon layer, patterning the polysilicon layer, implanting barrier diffusion, trimming the photoresist layer on the polysilicon layer, etching the polysilicon layer by using the trimmed photoresist layer as mask, then removing the photoresist. After removing the photoresist, a nitride layer is filled in the patterned polysilicon layer openings. The etching steps are preformed by using the nitride layer as a mask. The polysilicon layer and part of the ONO layer are removed, and the gate oxide layer is exposed. Two isolated ONO segments are formed by these etching steps. A polysilicon gate is then formed on the gate oxide layer.